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A RELIABLE SWITCH LADDER MULTI-LEVEL INVERTER

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ABSTRACT: In this paper, a multi-level inverter (MLI) based on switch ladder topology is presented. In conventional MLI, the arrangement of power semi-conductor switches is in series and a large number of switches conduct at the same time. Moreover, if one switch fails to conduct, the whole output voltage collapses. Thus, the conventional MLIs are less reliable and they have high on-state voltage drop. As compared to the conventional MLIs, the switch ladder inverter topology presented in this paper deploys parallel arrangement of controlled switches. Switch ladder topology uses less number of controlled switches, gate drive circuits and diodes. Therefore, it has minimal on-state voltage drop, less conduction losses, less switching complexity and high reliability. MATLAB/Simulink platform is chosen to simulate the proposed Switch Ladder Multi-Level Inverter. The viability of the proposed inverter has been proven through hardware results as well.

Keywords: Multilevel Inverter, Switch ladder topology, High reliability, Less conduction losses

INTRODUCTION

For the last few decades, Multilevel Inverters (MLIs) have penetrated in the industry where they have been habituated to a large number of practical applications. Indeed, one of the many advantages of multilevel inverters is that they can be interfaced with renewable energy sources such as photovoltaic cells, wind energy and fuel cells (Rodriguez *et al.*, 2002). As their output voltage is closer to the sinusoidal voltage waveform, they have less Total Harmonic Distortion (THD), high efficiency and low electromagnetic interference (EMI) due to low switching frequency (Lai and Peng, 1996). MLIs are utilized in high power and low/medium voltage applications.

Multilevel inverter was first introduced in 1979. It began as a three level inverter (Sozer and Torrey, 2009). Since then, numerous topologies have been introduced. The first topology proposed was called cascaded H-bridge (CHB) (Agrawal and Jain, 2017). The second topology proposed by Nabae in 1981, was named neutral-point-clamped (NPC) (Babaei and Hosseini, 2009). For NPC-MLIs, the crucial problem lies in the voltage unbalance of series connected dc link capacitors (Alishah *et al.*2014). In third topology named Flying Capacitor (FC), the number of diodes and switches increase with the increase in voltage levels (Nabae *et al.*, 1981). FC-MLI faces the same problem of voltage unbalancing of capacitors as NPC-MLI (Meynard *et al.*, 2002). As compared to diode-clamped and flying capacitor topology, CHB-MLI uses least number of components and avoids extra clamping diodes and voltage balancing capacitors (Samadaei *et al.*, 2016). The applications of cascaded inverter are limited by a major disadvantage i.e. in cascaded configuration, failure of a single switch failure leads to the failure of the whole inverter operation (Kouro *et al.*, 2010). However, the restraining factor associated with the all the conventional topologies is the requirement of large number of power semi-conductor switches, gate driver circuits and auxiliary components with the increase in each voltage level (Kuriakose and Anooja, 2014). As the conventional topologies are connected in series/cascaded form, the failure of a single switch will cause the whole output voltage to collapse. Moreover, the series connected switches have high on-state voltage drop leading to increased conduction losses. For this purpose, a reliable inverter having reduced number of switches and minimal on-state voltage drop is proposed in this paper.

MATERIALS AND METHODS

Three cases of MLIs based on switch ladder topology are discussed in this paper, which consists of bidirectional switches and DC sources of same magnitude. All the switches are connected in a parallel connection. The converter requires bidirectional switches with high-voltage capability, medium switching and the ability to conduct current in both directions. For this purpose, IGBTs with anti-parallel diodes are used.

Switch ladder multilevel inverter (Case-1): The basic structure of switch ladder logic based multi-level inverter (SL-MLI) is shown in Figure 1. It has seven levels. This inverter consists of bidirectional switches with antiparallel diodes. It has two legs; positive and negative. Positive leg consists of parallel connected switches ranging from SP & S3 to S1 (SN) switches while negative leg consists of SN and S4 (SN+1) to S6 (S2N) where N represents the number of DC sources.

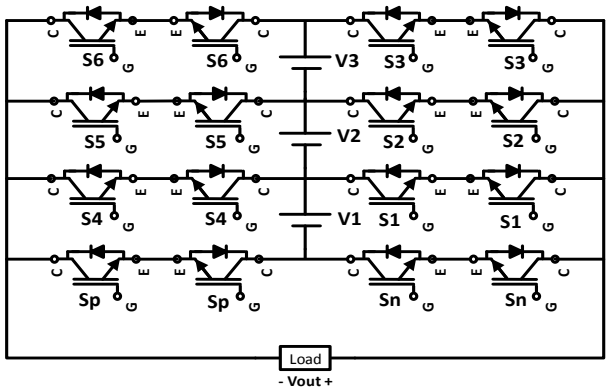

Figure-1: Basic switch ladder multilevel inverter proposed structure.

The switching strategy is shown in Table 1. For a seven level inverter, number of DC sources are three i.e. N=3. For the positive half cycle, the positive leg conducts and negative leg remains in the off - state and vice-versa. When SN switch conducts, it gives a zero voltage level; S1 gives V1 and S2 gives the addition of voltages V1 and V2 i.e. V1 + V2 on the output. Likewise, with every increasing voltage level, voltage from previous level is added. The fundamental advantage of this topology is that the failure of any switch will not cause the entire output voltage to be nil, but the voltage level across that particular failed switch will become zero. As only four switches conduct at the same time in each cycle, inverter has a minimum on-state voltage drop and power loss.

Table 1: Basic SL-MLI Switching Pattern For Positive Half Cycle. (Referred To Figure 1).

Sp	Sn	S1	S2	S3	S4 to S6	Output
1	1	0	0	0	0	0
1	0	1	0	0	0	V1
1	0	0	1	0	0	V1+V2
1	0	0	0	1	0	V1+V2+V3
1	0	0	0	1	0	V1+V2+V3
1	0	0	1	0	0	V1+V2
1	0	1	0	0	0	V1
1	1	0	0	0	0	0

Switch ladder Multilevel Inverter with Reduced Switches (Case-II): The multilevel-inverter proposed in Figure 1 consists of large number of switches. To reduce the number of switches, a new topology is proposed i.e. Switch Ladder Multilevel Inverter with reduced switches. It consists of two parts: positive leg of previously presented inverter i.e. Basic SL-MLI (basic unit) and one H-bridge cell (polarity changer) (Kuriakose and Anooja, 2014). The other half leg of fundamental SL-MLI is removed for the purpose of reducing the switches in this topology.

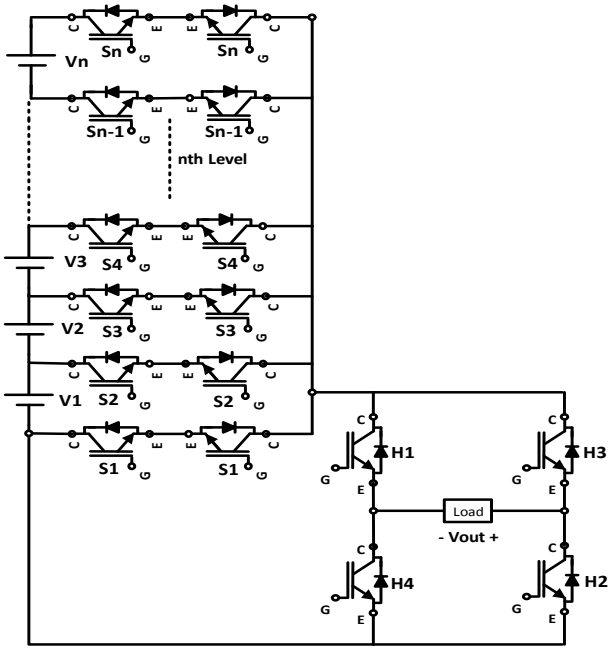

Figure-2 Switch ladder multilevel inverter with reduced number of switches.

The operation of this inverter is similar to a single-phase H-bridge inverter. The basic unit produces the waveform in positive polarity in two half period (Kuriakose and Anooja, 2014). The H-bridge inverter is used as a polarity changer in this topology. It inverts the waveform produced by the basic unit, thus, producing the waveform in both polarities (Kuriakose and Anooja, 2014). The number of voltage levels is given as

$$L = 2n + 1 \quad \text{(i)}$$

Where n is the number of DC-voltage sources. The foremost advantage of this topology is that it uses reduced number of switches as compared to the basic topology of SL-MLI. During each cycle, only four switches conduct at any given time resulting in minimal conduction and switching losses.

Reliable Switch-Ladder Multilevel Inverter (Case-III): A reliable multilevel inverter based on switch ladder logic is shown in Fig. 3. MLI proposed in case-II is further made reliable by providing at-least two stand-by switches to each conducting switch. In Figure 3 (a), S5 is the conducting switch while S3 and S8 are kept on and in standby mode to support S5. The direction of current is also shown. The output voltage at this level will be the addition of voltages V1 and V2 i.e. V1+V2. When switch S5 conducts, the diode of switch S6 becomes forward biased and provides a path for current to flow through it, which in turn causes the S3 diode to be reverse-biased. Switch S3 still remains in on condition, which means S3 is considered to be in standby mode. The reason for having stand-by switches is that if a higher switch fails to conduct due to any problem, the current will pass through the lower stand-by switch and lower switch diode will get

forward biased. Thus, the system will not collapse and will continue to facilitate the user without any interruption. The demonstration of this method is shown in Fig. 3 (b): when S5 fails to conduct, the voltage is jumped to a previous level as the standby switch S3 turns on and provides a path for current to flow through it. Instead of achieving nil voltage at the output, a previous voltage level i.e. V1 is achieved. In this way, the reliability of inverter is notably increased.

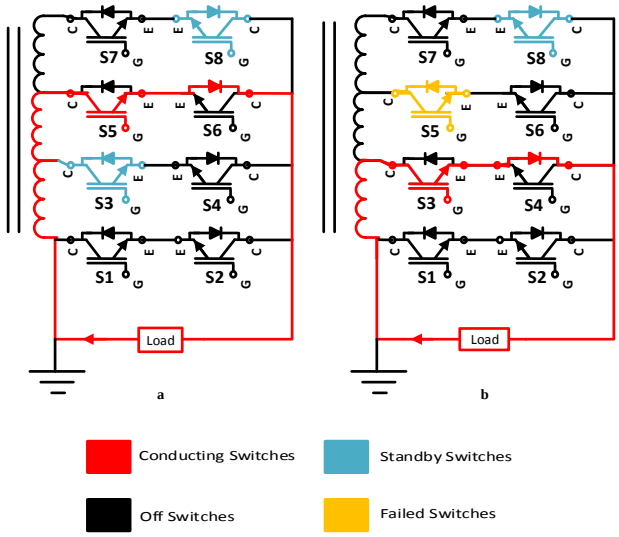

Figure-3: Reliable Switch ladder multilevel inverter.

RESULTS AND DISCUSSION

In order to check the feasibility of the proposed inverter, simulations are carried out on MATLAB/ SIMULINK of the three cases discussed in the paper. For practical implementation, a prototype of switch ladder multilevel inverter with reduced switches (Case-II) is constructed for 5 levels or 9 levels peak-peak.

Simulation Results (Case-1): A 20-level (zero to peak in half cycle) MLI based on Figure 3.1 with 19 DC sources i.e. N=19 is simulated. Here "N" represents the number of DC sources. Figures 4.1 and 4.2 show the 20-level output voltage and output current of Basic SL-MLI running under normal conditions respectively. In figure 4.3, switch S5 is made to fail in an open circuit behavior to depict the failure of a switch in a practical environment. As explained before, the failure of a switch does not affect the whole output voltage, instead the voltage-level across failed switch S5 jumps to zero. In Fig. 4.3, it can be seen that the area under the curve does not remain same when switch S5 fails. A demerit of this inverter is that a dc offset is introduced into the system when a switch fails to conduct.

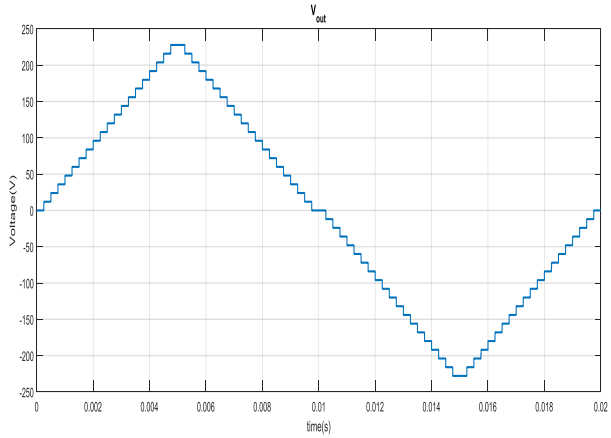

Figure-4.1: Output voltage of 'Basic switch ladder multilevel inverter' under normal conditions.

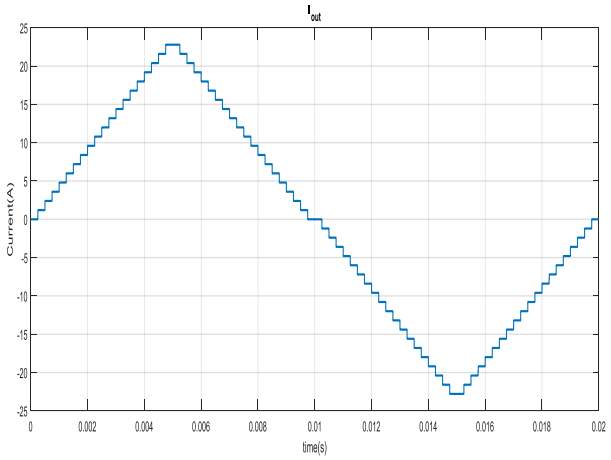

Figure-4.2: Output current of 'Basic Switch ladder multilevel inverter' under normal conditions.

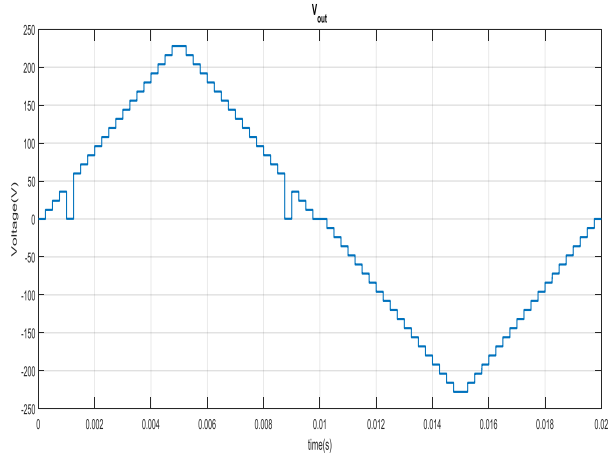

Figure-4.3: Output voltage of 'Basic Switch ladder multilevel inverter' when switch S5 fails.

Simulation Results(Case-II): A 20-level MLI based on Figure 3.2 with 19 DC sources i.e. N=19 (where N

represents number of DC sources) is simulated. In figure 4.4, switch S5 is made to fail to depict the failure of a switch. The results show that instead of getting the whole output zero, the voltage level across that failed switch S5 becomes zero. As compared to the basic SL-MLI (case-I) topology, the area under the curve for case-II, remains same when a switch fails to conduct i.e. $V_{avg} = 0$.

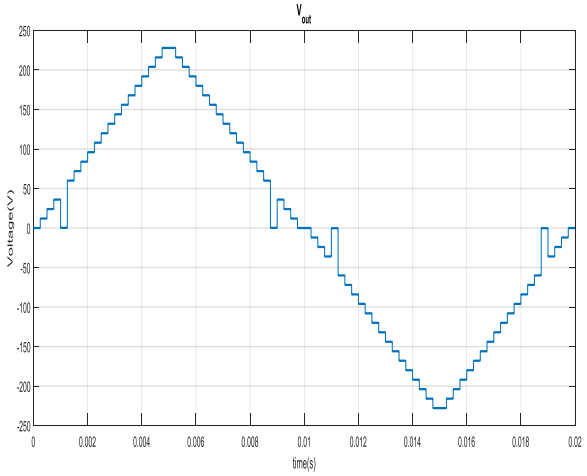

Figure-4.4: Output voltage of 'Switch ladder multilevel inverter with reduced switches' when switch S5 fails.

Simulation Result(Case-III): A 20 level reliable SL-MLI referred to Figure 3 is simulated. Figure 4.5 shows the output voltage of Reliable SL-MLI running under normal conditions. Figures 4.6 and 4.7 illustrate output voltage and current when switch S5 fails respectively. The presented results verify that the entire output voltage is not affected by the failure of a switch but the voltage across the failed switch jumps to a lower level and not to zero. Therefore, the presented results show that the service of the inverter is not interrupted due to the failure of a switch. This makes the proposed inverter more reliable than the previously presented topologies (Case-III, Figure 3).

Hardware Results (Case-II): For practical implementation, a prototype of switch ladder multilevel inverter with reduced switches as shown in figure 5.1 (Case-2) was constructed for 5 levels. The inverter delivers power to a test load of 25W. The results shown are captured from a digital oscilloscope. Figure 5.2 shows an output voltage waveform under normal conditions. Figure 5.3 illustrates the failure of switch S5 and its neighbor switch in an open circuit behavior. As expected, and discussed before, the entire output voltage doesn't collapse instead the voltage across the failed switch S5 becomes nil and the system continues its service. Similarly, Figure 5.4 depicts the failure of switch S3.

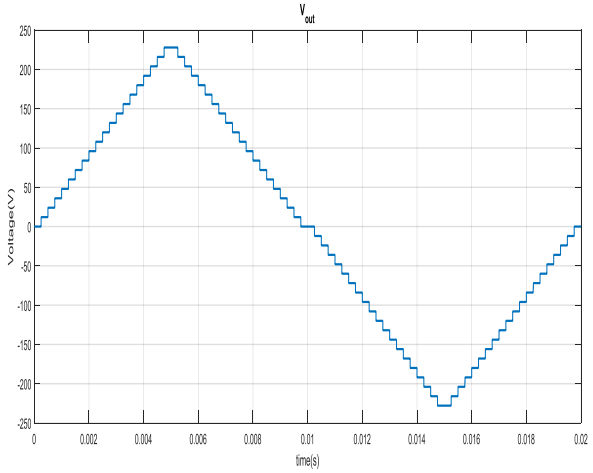

Figure-4.5: Output voltage of 'Reliable Switch Ladder Multilevel Inverter' under normal conditions.

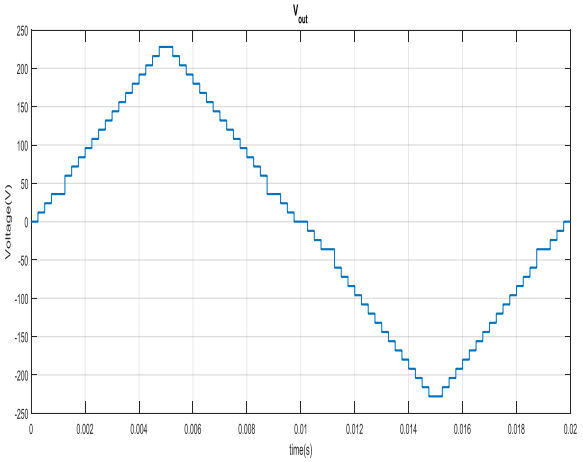

Figure-4.6: Reliable SL-MLI output voltages when switch S5 fails.

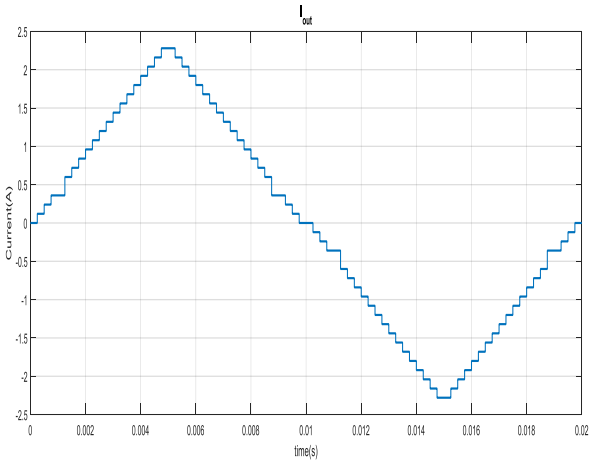

Figure-4.7: Reliable SL-MLI output current when switch S5 fails.

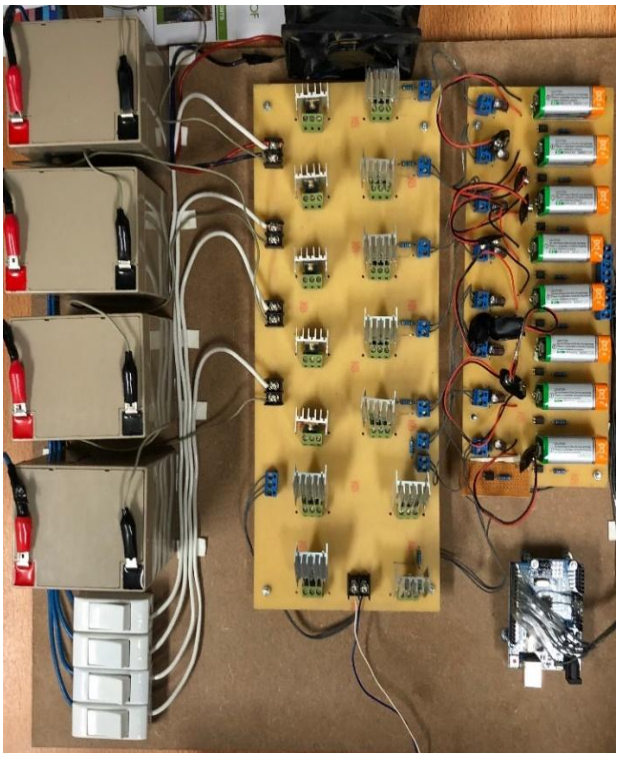

Figure-5.1. Prototype of SL-MLI with reduce switches.

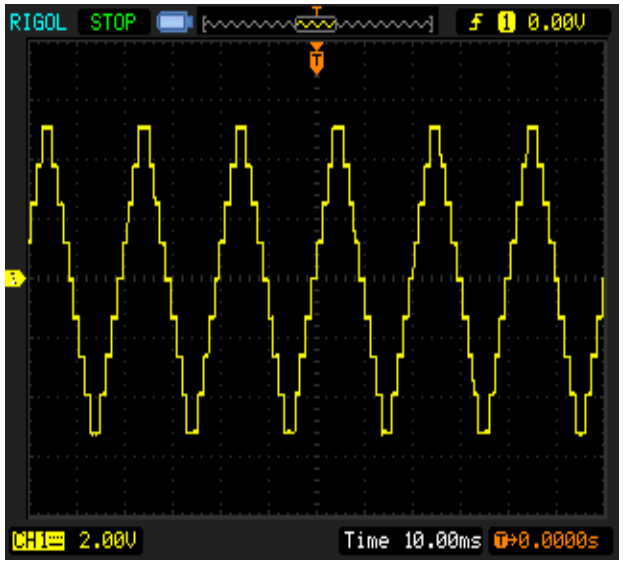

Figure-5.2: Output voltage of 'Switch Ladder Multilevel Inverter' with reduced switches under normal conditions.

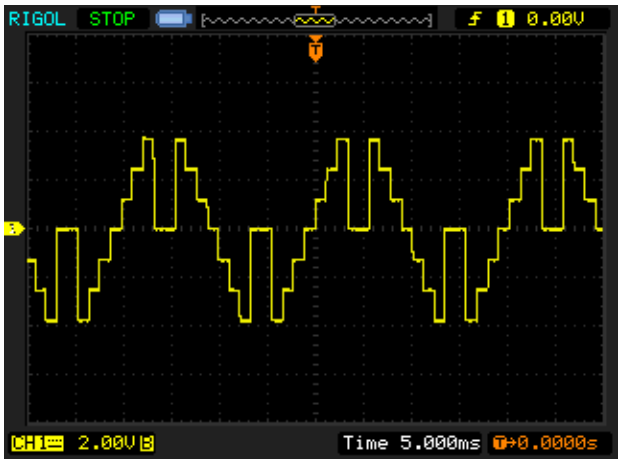

Figure-5.3: Output voltage of 'Switch Ladder Multilevel Inverter with reduced switches' when switch S5 fails.

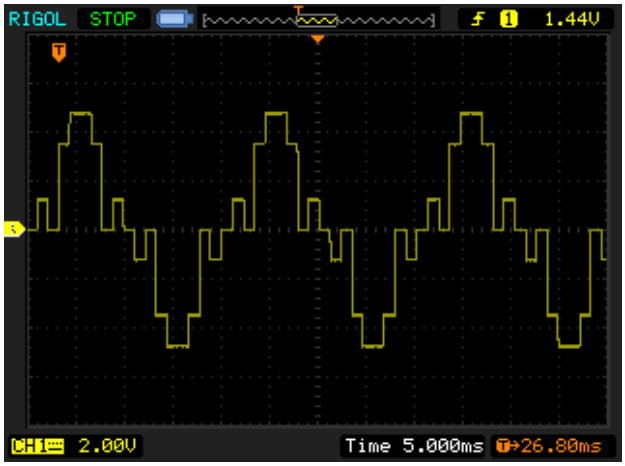

Figure-5.4: Output voltage of 'Switch Ladder Multilevel Inverter with reduced switches' when switch S3 fails.

Conclusion: A reliable multilevel inverter with reduced switches based on switch ladder topology is presented in this paper. The proposed inverter with reduced switches and auxiliary components has small size, less switching complexity and less cost. The parallel operation of controlled switches increases the reliability of the proposed inverter. In previous topologies like cascaded H-Bridge inverter, current only conducts when all switches of the inverter are on, but in the proposed topology due to parallel operation of switches, each voltage level can provide the individual path for the current to flow. The results prove that in the proposed inverter, if a higher switch fails, the output voltage doesn't jump to zero; instead it jumps to a previous voltage-level. In this way, the reliability of inverter is immensely increased.

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